

CPLD Specification

80x100GbE Switch

AS7926-80XK

Version: 1.0

Revision History

Rev.	Date	Author	Revision Description
V 1.0	8/29/2019		Initial OCP release

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1. CPLD overview

1.1. Fan CPLD Architecture

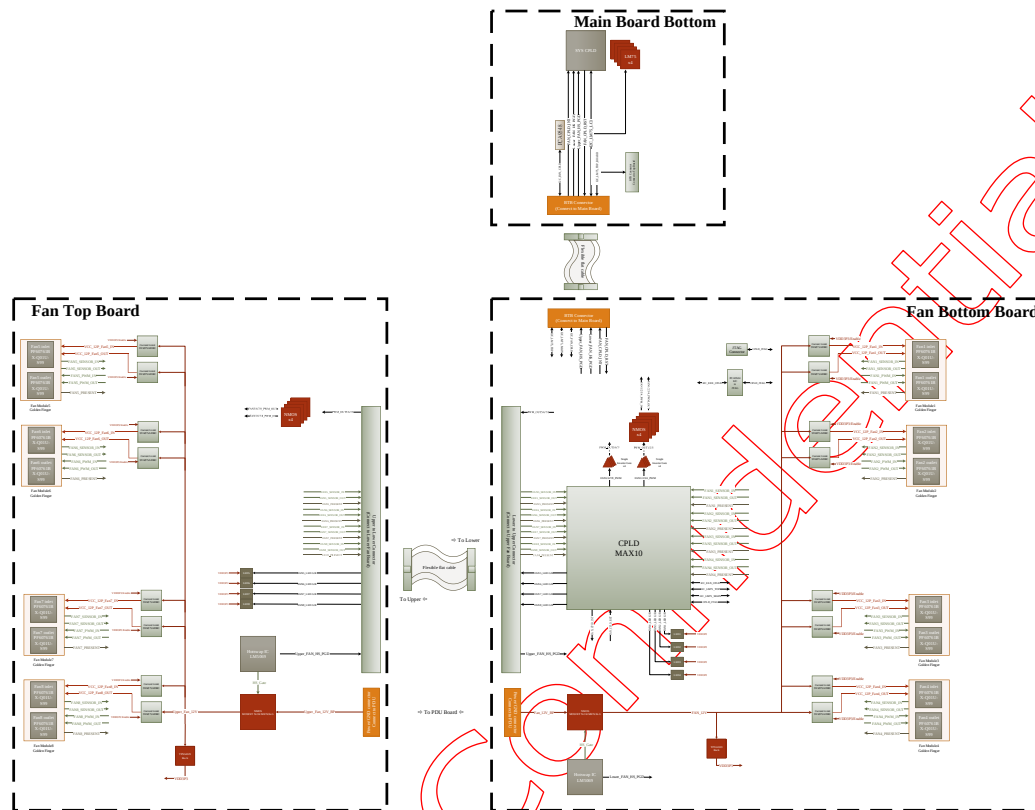


Figure 1-1 Fan Board Top/Bottom Block Diagram

CPU can access FAN CPLD via I2C interface to get the fan status.

The Fan CPLD has the register to control Fan PWM signal for fan speed control, and the counter for fan speed reporting. There is also fan power control to enable/ disable Fan power rail.

The CPLD will detect fan speed to check fan status if any issue. And CPLD will inform CPU by fan interrupt signal if there has fan fail occur or watchdog time out.

The fan LED will report the fan status via Red/ Green LED.

The watchdog timer is the thermal protection to avoid the CPU hang up. If watchdog timer count to zero, Fan CPLD will be pull-up the Fan speeds for system thermal protection.

Fan CPLD has 2 I2C master interfaces to connect to LM75s, TMP432 and System CPLD

of Main Board Top/Bottom. Fan CPLD needs to get temperature information repetitive on every I2C master interface and put what it gets into Temperature Register. The I2C master channel that connects to Main Board Top gets 7 thermal values which are from LM75s, TMP432 and the System CPLD, and the other I2C master channel that connects to Main Board Bottom gets 9 thermal values which are from LM75s, TMP432 and System CPLD. For LM75, The I2C device address is 0x4D, 0x4E, 0x4F and 0x4B. The device address of system CPLD is 0x60 and the device address of TMP432 is 0x4C. The thermal information offset is 0x30 for CPU and 0x31 for MAC.

To Read TMP432, please follow the description showed as below.

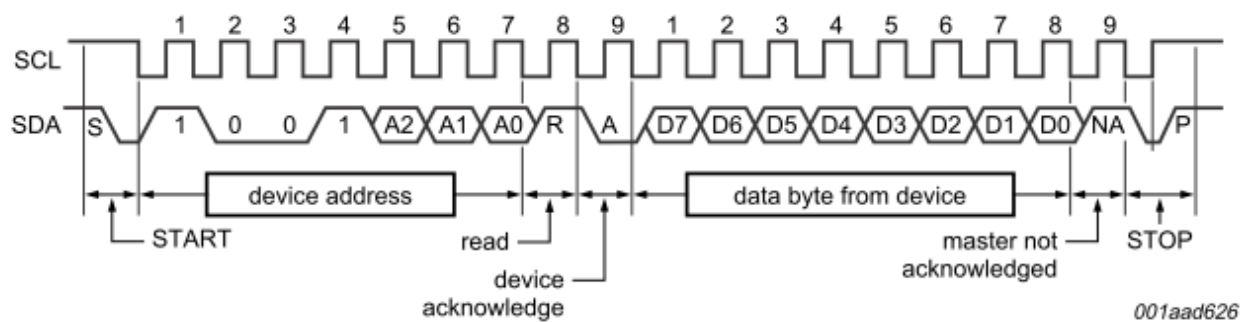
There are three temperature sensing channels in TMP432, one is the local channel, and the other two are the remote channels. Each channel uses two bytes to represent the temperature data, the high byte stores the temperature with 1 degree C resolution, and the low byte stores the temperature with the higher measurement resolution.

There are two modes for the different temperature sensing range, one is the “Standard mode”, its range is 0 degree C to 127 degree C, and the other mode is “Extended mode”, its sensing range is -64 degree C to 191 degree C. These two modes can be switched by changing bit 2 of Configuration Register 1 from low to high.

When the Fan CPLD gets the temperature data from the TMP432, it should be subtracted 64 degree C from the value of the temperature data (decimal value), and for the value after subtracting, it is the true temperature which is sensed by the TMP432. When the Fan CPLD gets those temperature data and puts those data in its own registers, it should be converted the format by using 2's complement encoding.

For the local channel, you can read the register 0x00 of TMP432 to get the measurement value of the local temperature. And for the other two channels, you can access the register 0x01(remote channel 1) and the register 0x23(remote channel 2) to get the sensing temperatures.

To Read LM75, please follow the format showed as below. And you need to write 0x80(-128) in to temp register if there did not have device acknowledge.



The temperature register definition of FAN CPLD matched to LM75 as 8 bits with 2's complement encoding. For CPU and ASIC temperatures, software running on CPU must translate temperatures read from the MAC ASIC and CPU into the LM75 format and place in defined locations inside System CPLD on the Main Board Bottom.

There are two fan speed control mechanisms, one controlled by FAN CPLD itself and the other controlled by external controller (C) via I2C slave interface. Can use GPIO_1 pin to select which mechanism we are going to use. If GPIO_1 is low, then the Fan speed will be controlled by external controller and value of "Watchdog Max PWM" register will copy to "FAN PWM" register when watchdog timer expired. If GPIO_1 is high, then the Fan speed will be controlled by Fan CPLD itself. This control mechanism can also be modified by change bit 7 of register 0x11 after system boot up.

The ZONE fan control algorithm is as follows when Fan speed controlled by CPLD itself:

1. Get Max value of each location on every board. For example, Max temp of ASIC is MAX(REG(0x51), Reg(0x59)). So there are 9 Max temp values on the Main Bottom board and 7 Max temp values on the Main Top board that we will get. They are MAX temp of CPU, ASIC, LM75_1, LM75_2, LM75_3, LM75_4, TMP432_1, TMP432_2, and TMP_432_3.
2. If all 15 temp values is 0x80(-128), that means no any cards be powered up so set fan speed to Min speed, else if any temp value bigger than 0x80 and current fan speed is Min speed then set fan to step1 speed
3. If current fan speed is setp1, then compare temp value with step1 high threshold. For example, CPU temp compare to 0xB0, LM75_1 compare to 0xC0... etc. If any temp value bigger than "step1 high threshold", then increase the fan speed to step2. Otherwise Keep fan speed as step1.
4. If current fan speed is setp2, then compare temp value with "step2 high/low

threshold". If any temp value bigger than "step2 high threshold", then increase the fan speed to Max. Else if all temp value lower than "step2 low threshold", then reduce the fan speed to step1. Otherwise Keep fan speed as step2

5. If current fan speed is Max, then compare temp value with "Max low threshold". If all temp value lower than "Max low threshold", then reduce the fan speed to step2. Otherwise Keep fan speed as Max.

Clock

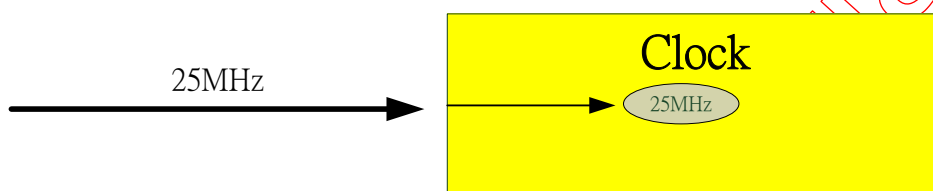


Figure 1-2 Fan Control Block Diagram

The CPLD reference clock is from 25MHz.

1.2. Fan Controller Register

※RO= Ready Only, R/W=Read & Write, NU=Not Use.

Address MB Mgmt	Register	R/W	Default value
0x00	Board Info	RO	0x03
0x01	CPLD version	RO	
0x04	Fan CPLD Reset	R/W	0x80
0x05	Interrupt Status	RO	0x80
0x06	Interrupt Mask	RO	0x00
0x0F	Fan Module Present	RO	0xFF
0x10	Fan Module Direction	NU	0x3F
0x11	Fan Module PWM	R/W	0x0F
0x12	Front Fan1 Module Speed	RO	
0x13	Front Fan2 Module Speed	RO	
0x14	Front Fan3 Module Speed	RO	
0x15	Front Fan4 Module Speed	RO	
0x16	Front Fan5 Module Speed	RO	

0x17	Front Fan6 Module Speed	RO	
0x18	Front Fan7 Module Speed	RO	
0x19	Front Fan8 Module Speed	RO	
0x1C	LED Display-1	R/W	0x00
0x1D	LED Display-2	R/W	0x00
0x22	Rear Fan1 Module Speed	RO	
0x23	Rear Fan2 Module Speed	RO	
0x24	Rear Fan3 Module Speed	RO	
0x25	Rear Fan4 Module Speed	RO	
0x26	Rear Fan5 Module Speed	RO	
0x27	Rear Fan6 Module Speed	RO	
0x28	Rear Fan7 Module Speed	RO	
0x29	Rear Fan8 Module Speed	RO	
0x30	Fan Module Power enable	R/W	0xFF
0x31	Watchdog timer	R/W	0x06
0x32	Watchdog Maximum PWM value	R/W	0x0F
0x33	Watchdog disable	R/W	0x01
0x34	Fan LED Debug	R/W	0x00
0x40	Min Fan Speed	R/W	PWM=0%??
0x41	Step1 Fan Speed	R/W	PWM=20%??
0x42	Step2 Fan Speed	R/W	PWM=50%??
0x43	Max Fan Speed	R/W	PWM=100%
0x50	CPU Temp	RO	0x80
0x51	Main Board Bottom ASIC Temp	RO	0x80
0x52	Main Board Bottom TMP432_1 Temp	RO	0x80
0x53	Main Board Bottom TMP432_2 Temp	RO	0x80
0x54	Main Board Bottom TMP432_3 Temp	RO	0x80
0x55	Main Board Bottom LM75_1 Temp	RO	0x80
0x56	Main Board Bottom LM75_2 Temp	RO	0x80
0x57	Main Board Bottom LM75_3 Temp	RO	0x80
0x58	Main Board Bottom LM75_4 Temp	RO	0x80
0x59	Main Board Top ASIC Temp	RO	0x80
0x60	Main Board Top LM75_1 Temp	RO	0x80
0x61	Main Board Top LM75_2 Temp	RO	0x80

0x62	Main Board Top LM75_3 Temp	RO	0x80
0x63	Main Board Top TMP432_1 Temp	RO	0x80
0x64	Main Board Top TMP432_2 Temp	RO	0x80
0x65	Main Board Top TMP432_3 Temp	RO	0x80
0xB0	CPU Step1 high threshold	R/W	
0xB1	CPU Step2 low threshold	R/W	
0xB2	CPU Step2 high threshold	R/W	
0xB3	CPU Max low threshold	R/W	
0xB4	ASIC Step1 high threshold	R/W	
0xB5	ASIC Step2 low threshold	R/W	
0xB6	ASIC Step2 high threshold	R/W	
0xB7	ASIC Max low threshold	R/W	
0xC0	LM75_1 Step1 high threshold	R/W	
0xC1	LM75_1 Step2 low threshold	R/W	
0xC2	LM75_1 Step2 high threshold	R/W	
0xC3	LM75_1 Max low threshold	R/W	
0xC4	LM75_2 Step1 high threshold	R/W	
0xC5	LM75_2 Step2 low threshold	R/W	
0xC6	LM75_2 Step2 high threshold	R/W	
0xC7	LM75_2 Max low threshold	R/W	
0xC8	LM75_3 Step1 high threshold	R/W	
0xC9	LM75_3 Step2 low threshold	R/W	
0xCA	LM75_3 Step2 high threshold	R/W	
0xCB	LM75_3 Max low threshold	R/W	
0xCC	LM75_4 Step1 high threshold	R/W	
0xCD	LM75_4 Step2 low threshold	R/W	
0xCE	LM75_4 Step2 high threshold	R/W	
0xCF	LM75_4 Max low threshold	R/W	
0xD0	TMP432_1 Step1 high threshold	R/W	
0xD1	TMP432_1 Step2 low threshold	R/W	
0xD2	TMP432_1 Step2 high threshold	R/W	
0xD3	TMP432_1 Max low threshold	R/W	
0xD4	TMP432_2 Step1 high threshold	R/W	
0xD5	TMP432_2 Step2 low threshold	R/W	

0xD6	TMP432_2 Step2 high threshold	R/W	
0xD7	TMP432_2 Max low threshold	R/W	
0xD8	TMP432_3 Step1 high threshold	R/W	
0xD9	TMP432_3 Step2 low threshold	R/W	
0xDA	TMP432_3 Step2 high threshold	R/W	
0xDB	TMP432_3 Max low threshold	R/W	

Table 1-1 Fan board CPLD I/O Register Table

1.2.1.Offset 0x00 Board Info (Read Only)

Bit	Name	R/W	Reset Value	Description
7:5	Version_ID[2:0]	R	000	000: R0A 001: R0B 100: R01 Others: Reserved
4:2	Reserved	N/A	NA	
1:0	Board_ID[1:0]	R	11	00: Reserved 01: ZZ project 10: Reserved 11: AO project

1.2.2.Offset 0x01 CPLD version (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	CPLD_ver[7:0]	R	0x00	CPLD version

1.2.3.Offset 0x04 Fan CPLD Reset (Read & Write)

Bit	Name	R/W	Reset Value	Description
7	CPU_FAN_CPLD_RST_N	R/W	1	1: CPLD is placed in normal operation state. 0: CPLD is placed in reset state.
6:0	Reserved	N/A	NA	

1.2.4.Offset 0x05 Interrupt Status (Read Only)

Bit	Name	R/W	Reset Value	Description
7	FAN_INT_L	R	1	1: No interrupt 0: There is INTR to CPU
6:0	Reserved	N/A	NA	

1.2.5.Offset 0x06 Interrupt Mask (Read Only)

Bit	Name	R/W	Reset Value	Description
7	MASK*Fan_interrupt	R/W	0	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
6:0	Reserved	N/A	NA	

1.2.6.Offset 0x0F Fan Module Present (Read Only)

Bit	Name	R/W	Reset Value	Description
7	FAN8_PRESENT	R	1	1: Fan8 isn't inserted 0: Fan8 is inserted
6	FAN7_PRESENT	R	1	1: Fan7 isn't inserted 0: Fan7 is inserted
5	FAN6_PRESENT	R	1	1: Fan6 isn't inserted 0: Fan6 is inserted
4	FAN5_PRESENT	R	1	1: Fan5 isn't inserted 0: Fan5 is inserted
3	FAN4_PRESENT	R	1	1: Fan4 isn't inserted 0: Fan4 is inserted
2	FAN3_PRESENT	R	1	1: Fan3 isn't inserted 0: Fan3 is inserted
1	FAN2_PRESENT	R	1	1: Fan2 isn't inserted 0: Fan2 is inserted
0	FAN1_PRESENT	R	1	1: Fan1 isn't inserted 0: Fan1 is inserted

1.2.7.Offset 0x11 Fan Module PWM (Read & Write)

Bit	Name	R/W	Reset Value	Description
7	FAN Speed control mechanisms	R/W	Pin B1 GPIO_1	0: Control by external controller 1: Control by CPLD automatic Need set 0x33[7] to unlock this register to change the value.
6:4	reserve	N/A	N/A	
3:0	FANn_PWM [3:0] ※(n = 1~8)	R/W	1111	The value of this field will be forced to 4 if a value less than 4 is written. 0100 : 5 x 6.25% = 31.5% duty cycle 0101 : 6 x 6.25% = 37.5% duty cycle 0110: 7 x 6.25% = 43.75% duty cycle 1110: 15 x 6.25% = 93.75% duty cycle 1111: 16 x 6.25% = 100% duty cycle

1.2.8.Offset 0x12 Front Fan1 Module Speed (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	FAN1_SENSOR_IN	R		0: Fan failed 1 ~ 255: the number of fan rotations in 600ms ⇒ Fan speed (RPM) = Reg_value * 100 EX: register value : 80 The RPM value is 80*100 = 8000

1.2.9.Offset 0x13 Front Fan2 Module Speed(Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	FAN2_SENSOR_IN	R		0: Fan failed 1 ~ 255: the number of fan rotations in 600ms ⇒ Fan speed (RPM) = Reg_value * 100 EX: register value : 80 The RPM value is 80*100 = 8000

1.2.10. Offset 0x14 Front Fan3 Module Speed (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	FAN3_SENSOR_IN	R		0: Fan failed 1 ~ 255: the number of fan rotations in 600ms $\Rightarrow$ Fan speed (RPM) = Reg_value * 100 EX: register value : 80 The RPM value is $80 * 100 = 8000$

1.2.11. Offset 0x15 Front Fan4 Module Speed (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	FAN4_SENSOR_IN	R		0: Fan failed 1 ~ 255: the number of fan rotations in 600ms $\Rightarrow$ Fan speed (RPM) = Reg_value * 100 EX: register value : 80 The RPM value is $80 * 100 = 8000$

1.2.12. Offset 0x16 Front Fan5 Module Speed (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	FAN5_SENSOR_IN	R		0: Fan failed 1 ~ 255: the number of fan rotations in 600ms $\Rightarrow$ Fan speed (RPM) = Reg_value * 100 EX: register value : 80 The RPM value is $80 * 100 = 8000$

1.2.13. Offset 0x17 Front Fan6 Module Speed (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	FAN6_SENSOR_IN	R		0: Fan failed 1 ~ 255: the number of fan rotations in 600ms $\Rightarrow$ Fan speed (RPM) = Reg_value * 100 EX: register value : 80 The RPM value is $80 * 100 = 8000$

1.2.14. Offset 0x18 Front Fan7 Module Speed (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	FAN7_SENSOR_IN	R		0: Fan failed 1 ~ 255: the number of fan rotations in 600ms $\Rightarrow$ Fan speed (RPM) = Reg_value * 100 EX: register value : 80 The RPM value is $80 \times 100 = 8000$

1.2.15. Offset 0x19 Front Fan8 Module Speed (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	FAN8_SENSOR_IN	R		0: Fan failed 1 ~ 255: the number of fan rotations in 600ms $\Rightarrow$ Fan speed (RPM) = Reg_value * 100 EX: register value : 80 The RPM value is $80 \times 100 = 8000$

1.2.16. Offset 0x1C LED Display-1 (Read & Write)

Bit	Name	R/W	Reset Value	Description
7	PWM1 for FAN1_LED_R	R/W	0	1: Fan1_LED is Red 0: off
6	PWM1 for FAN1_LED_G	R/W	0	1: Fan1_LED is Green 0: off
5	PWM2 for FAN2_LED_R	R/W	0	1: Fan2_LED is Red 0: off
4	PWM2 for FAN2_LED_G	R/W	0	1: Fan2_LED is Green 0: off
3	PWM3 for FAN3_LED_R	R/W	0	1: Fan3_LED is Red 0: off
2	PWM3 for FAN3_LED_G	R/W	0	1: Fan3_LED is Green 0: off
1	PWM4 for	R/W	0	1: Fan4_LED is Red

	FAN4_LED_R			0: off
0	PWM4 for FAN4_LED_G	R/W	0	1: Fan4_LED is Green 0: off

1.2.17. Offset 0x1D LED Display-2 (Read & Write)

Bit	Name	R/W	Reset Value	Description
7	PWM5 for FAN5_LED_R	R/W	0	1: Fan5_LED is Red 0: off
6	PWM5 for FAN5_LED_G	R/W	0	1: Fan5_LED is Green 0: off
5	PWM6 for FAN6_LED_R	R/W	0	1: Fan6_LED is Red 0: off
4	PWM6 for FAN6_LED_G	R/W	0	1: Fan6_LED is Green 0: off
3	PWM7 for FAN7_LED_R	R/W	0	1: Fan7_LED is Red 0: off
2	PWM7 for FAN7_LED_G	R/W	0	1: Fan7_LED is Green 0: off
1	PWM8 for FAN8_LED_R	R/W	0	1: Fan8_LED is Red 0: off
0	PWM8 for FAN8_LED_G	R/W	0	1: Fan8_LED is Green 0: off

1.2.18. Offset 0x22 Rear Fan1 Module Speed (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	FAN1_SENSOR_OUT	R	0	0: Fan failed 1 ~ 255: the number of fan rotations in 600ms ⇒ Fan speed (RPM) = Reg_value * 100 EX: register value : 80 The RPM value is 80*100 = 8000

1.2.19. Offset 0x23 Rear Fan2 Module Speed (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	FAN2_SENSOR_OUT	R	0	0: Fan failed 1 ~ 255: the number of fan rotations in 600ms $\Rightarrow$ Fan speed (RPM) = Reg_value * 100 EX: register value : 80 The RPM value is $80 \times 100 = 8000$

1.2.20. Offset 0x24 Rear Fan3 Module Speed (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	FAN3_SENSOR_OUT	R	0	0: Fan failed 1 ~ 255: the number of fan rotations in 600ms $\Rightarrow$ Fan speed (RPM) = Reg_value * 100 EX: register value : 80 The RPM value is $80 \times 100 = 8000$

1.2.21. Offset 0x25 Rear Fan4 Module Speed (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	FAN4_SENSOR_OUT	R	0	0: Fan failed 1 ~ 255: the number of fan rotations in 600ms $\Rightarrow$ Fan speed (RPM) = Reg_value * 100 EX: register value : 80 The RPM value is $80 \times 100 = 8000$

1.2.22. Offset 0x26 Rear Fan5 Module Speed (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	FAN5_SENSOR_OUT	R	0	0: Fan failed 1 ~ 255: the number of fan rotations in 600ms $\Rightarrow$ Fan speed (RPM) = Reg_value * 100 EX: register value : 80 The RPM value is $80 \times 100 = 8000$

1.2.23. Offset 0x27 Rear Fan6 Module Speed (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	FAN6_SENSOR_OUT	R	0	0: Fan failed 1 ~ 255: the number of fan rotations in 600ms ⇒ Fan speed (RPM) = Reg_value * 100 EX: register value : 80 The RPM value is 80*100 = 8000

1.2.24. Offset 0x28 Rear Fan7 Module Speed (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	FAN7_SENSOR_OUT	R	0	0: Fan failed 1 ~ 255: the number of fan rotations in 600ms ⇒ Fan speed (RPM) = Reg_value * 100 EX: register value : 80 The RPM value is 80*100 = 8000

1.2.25. Offset 0x29 Rear Fan8 Module Speed (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	FAN8_SENSOR_OUT	R	0	0: Fan failed 1 ~ 255: the number of fan rotations in 600ms ⇒ Fan speed (RPM) = Reg_value * 100 EX: register value : 80 The RPM value is 80*100 = 8000

1.2.26. Offset 0x30 Fan Module Power enable (Read & Write)

Bit	Name	R/W	Reset Value	Description
7	EN_FAN8	R/W	1	1: Enable the fan Power 0: Disable the fan power
6	EN_FAN7	R/W	1	1: Enable the fan Power 0: Disable the fan power

5	EN_FAN6	R/W	1	1: Enable the fan Power 0: Disable the fan power
4	EN_FAN5	R/W	1	1: Enable the fan Power 0: Disable the fan power
3	EN_FAN4	R/W	1	1: Enable the fan Power 0: Disable the fan power
2	EN_FAN3	R/W	1	1: Enable the fan Power 0: Disable the fan power
1	EN_FAN2	R/W	1	1: Enable the fan Power 0: Disable the fan power
0	EN_FAN1	R/W	1	1: Enable the fan Power 0: Disable the fan power

1.2.27. Offset 0x31 Watchdog timer (Read & Write)

Bit	Name	R/W	Reset Value	Description
7:0	Watchdog timer	R/W	0x06	A countdown timer with 1 second resolution. Default value is 6 sec.

1.2.28. Offset 0x32 Watchdog Maximum PWM value (Read & Write)

Bit	Name	R/W	Reset Value	Description
7:4	reserve	NA	NA	
3:0	Watchdog Maximum PWM value	R/W	1111	This register's contents will be copied to the PWM register when the watchdog timer expires (WD == 0) The value of this field will be forced to 4 if a value less than 4 is written. 0100 : 5 x 6.25% = 31.5% duty cycle 0101 : 6 x 6.25% = 37.5% duty cycle 0110: 7 x 6.25% = 43.75% duty cycle 1110: 15 x 6.25% = 93.75% duty cycle 1111: 16 x 6.25% = 100% duty cycle

1.2.29. Offset 0x33 Watchdog disable (Read & Write)

Bit	Name	R/W	Reset Value	Description
7	Control mechanism lock	R/W	0	0: Lock control mechanism change 1: Unlock control mechanism change
6:1	reserve	NA	NA	
0	Watchdog disable	R/W	1	1: Enable the watchdog timer 0: Disable the watchdog timer

1.2.30. Offset 0x34 Fan LED Debug (Read & Write)

Bit	Name	R/W	Reset Value	Description
7	LED_Debug_mode	R/W	0	1:LED debug mode on 0:LED debug mode off
6:0	Reserve	N/A	N/A	

1.2.31. Offset 0x40 Min Fan Speed (Read & Write)

Bit	Name	R/W	Reset Value	Description
7:4	Reserve	N/A	N/A	
3:0	Min Fan Speed	R/W	TBD 0%?	Minimum Fan speed. Will use this value to replace FAN PWM register value when there did not have any card present.

1.2.32. Offset 0x41 Step 1 Fan Speed (Read & Write)

Bit	Name	R/W	Reset Value	Description
7:4	Reserve	N/A	N/A	
3:0	Step1 Fan Speed	R/W	TBD 20%?	Step 1 Fan speed. Will use this value to replace FAN PWM register value when thermal value within Step 1 threshold range.

1.2.33. Offset 0x42 Step 2 Fan Speed (Read & Write)

Bit	Name	R/W	Reset Value	Description
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7:4	Reserve	N/A	N/A	
3:0	Step 2 Fan Speed	R/W	TBD 50%?	Step 2 Fan speed. Will use this value to replace FAN PWM register value when thermal value within Step 2 threshold range.

1.2.34. Offset 0x43 Max Fan Speed (Read & Write)

Bit	Name	R/W	Reset Value	Description
7:4	Reserve	N/A	N/A	
3:0	Max Fan Speed	R/W	TBD 100%?	Maximum Fan speed. Will use this value to replace FAN PWM register value when thermal value within Max threshold range.

1.2.35. Offset 0x50 CPU Temp (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	CPU temperature	R	0x80	CPU temperature value with 2's complement. This value gets from System CPLD 0x30 register.

1.2.36. Offset 0x51 Main Board Bottom ASIC Temp (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	Main Board Bottom ASIC temperature	R	0x80	Main Board Bottom ASIC temperature value with 2's complement. This value gets from System CPLD 0x31 register.

1.2.37. Offset 0x52 Main Board Bottom TMP432_1 Temp (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	Main Board Bottom TMP432_1 temperature	R	0x80	Main Board Bottom LM75a temperature value with 2's complement. This value gets from Main Board Bottom LM75a.

1.2.38. Offset 0x53 Main Board Bottom TMP432_2 Temp (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	Main Board Bottom TMP432_2 temperature	R	0x80	Main Board Bottom LM75a temperature value with 2's complement. This value gets from Main Board Bottom LM75a.

1.2.39. Offset 0x54 Main Board Bottom TMP432_3 Temp (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	Main Board Bottom TMP432_3 temperature	R	0x80	Main Board Bottom LM75a temperature value with 2's complement. This value gets from Main Board Bottom LM75a.

1.2.40. Offset 0x55 Main Board Bottom LM75_1 Temp (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	Main Board Bottom LM75_1 temperature	R	0x80	Main Board Bottom LM75b temperature value with 2's complement. This value gets from Main Board Bottom LM75b.

1.2.41. Offset 0x56 Main Board Bottom LM75_2 Temp (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	Main Board Bottom LM75_2 temperature	R	0x80	Main Board Bottom LM75c temperature value with 2's complement. This value gets from Main Board Bottom LM75c.

1.2.42. Offset 0x57 Main Board Bottom LM75_3 Temp (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	Main Board Bottom LM75_3 temperature	R	0x80	Main Board Bottom LM75d temperature value with 2's complement. This value gets from Main Board Bottom LM75d.

1.2.43. Offset 0x58 Main Board Bottom LM75_4 Temp (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	Main Board Bottom LM75_4 temperature	R	0x80	Main Board Bottom LM75d temperature value with 2's complement. This value gets from Main Board Bottom LM75d.

1.2.44. Offset 0x59 Main Board Top ASIC Temp (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	Main Board Top ASIC temperature	R	0x80	Main Board Top ASIC temperature value with 2's complement. This value gets from System CPLD 0x32 register.

1.2.45. Offset 0x60 Main Board Top LM75_1 Temp (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	Main Board Top LM75_1 temperature	R	0x80	Main Board Top LM75a temperature value with 2's complement. This value gets from Main Board Top LM75a.

1.2.46. Offset 0x61 Main Board Top LM75_2 Temp (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	Main Board Top LM75_2 temperature	R	0x80	Main Board Top LM75b temperature value with 2's complement. This value gets from Main Board Top LM75b.

1.2.47. Offset 0x62 Main Board Top LM75_3 Temp (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	Main Board Top LM75_3 temperature	R	0x80	Main Board Top LM75c temperature value with 2's complement. This value gets from Main Board Top LM75c.

1.2.48. Offset 0x63 Main Board Top TMP432_1 Temp (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	Main Board Top TMP432_1 temperature	R	0x80	Main Board Bottom LM75a temperature value with 2's complement. This value gets from Main Board Bottom LM75a.

1.2.49. Offset 0x64 Main Board Top TMP432_2 Temp (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	Main Board Top TMP432_2 temperature	R	0x80	Main Board Bottom LM75a temperature value with 2's complement. This value gets from Main Board Bottom LM75a.

1.2.50. Offset 0x65 Main Board Top TMP432_3 Temp (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	Main Board Top TMP432_3 temperature	R	0x80	Main Board Bottom LM75a temperature value with 2's complement. This value gets from Main Board Bottom LM75a.

1.2.51. Offset 0xB0 CPU Step 1 High threshold (Read & Write)

Bit	Name	R/W	Reset Value	Description
7:0	CPU Step 1 High threshold	R/W	TBD	CPU Step 1 High threshold temperature value with 2's complement.

1.2.52. Offset 0xB1 CPU Step 2 Low threshold (Read & Write)

Bit	Name	R/W	Reset Value	Description
7:0	CPU Step 2 Low threshold	R/W	TBD	CPU Step 2 Low threshold temperature value with 2's complement.

1.2.53. Offset 0xB2 CPU Step 2 High threshold (Read & Write)

Bit	Name	R/W	Reset Value	Description
7:0	CPU Step 2 High threshold	R/W	TBD	CPU Step 2 High threshold temperature value with 2's complement.

1.2.54. Offset 0xB3 CPU Max Low threshold (Read & Write)

Bit	Name	R/W	Reset Value	Description
7:0	CPU Max Low threshold	R/W	TBD	CPU Max Low threshold temperature value with 2's complement.

1.2.55. Offset 0xB4 ASIC Step 1 High threshold (Read & Write)

Bit	Name	R/W	Reset Value	Description
7:0	ASIC Step 1 High threshold	R/W	TBD	ASIC Step 1 High threshold temperature value with 2's complement.

1.2.56. Offset 0xB5 ASIC Step 2 Low threshold (Read & Write)

Bit	Name	R/W	Reset Value	Description
7:0	ASIC Step 2 Low threshold	R/W	TBD	ASIC Step 2 Low threshold temperature value with 2's complement.

1.2.57. Offset 0xB6 ASIC Step 2 High threshold (Read & Write)

Bit	Name	R/W	Reset Value	Description
7:0	ASIC Step 2 High threshold	R/W	TBD	ASIC Step 2 High threshold temperature value with 2's complement.

1.2.58. Offset 0xB7 ASIC Max Low threshold (Read & Write)

Bit	Name	R/W	Reset Value	Description
7:0	ASIC Max Low threshold	R/W	TBD	ASIC Max Low threshold temperature value with 2's complement.

1.2.59. Offset 0xC0 LM75_1 Step 1 High threshold (Read & Write)

Bit	Name	R/W	Reset Value	Description
7:0	LM75_1 Step 1 High threshold	R/W	TBD	LM75a Step 1 High threshold temperature value with 2's complement.

1.2.60. Offset 0xC1 LM75_1 Step 2 Low threshold (Read & Write)

Bit	Name	R/W	Reset Value	Description
7:0	LM75_1 Step 2 Low threshold	R/W	TBD	LM75a Step 2 Low threshold temperature value with 2's complement.

1.2.61. Offset 0xC2 LM75_1 Step 2 High threshold (Read & Write)

Bit	Name	R/W	Reset Value	Description
7:0	LM75_1 Step 2 High threshold	R/W	TBD	LM75a Step 2 High threshold temperature value with 2's complement.

1.2.62. Offset 0xC3 LM75_1 Max Low threshold (Read & Write)

Bit	Name	R/W	Reset Value	Description
7:0	LM75_1 Max Low threshold	R/W	TBD	LM75a Max Low threshold temperature value with 2's complement.

1.2.63. Offset 0xC4 LM75_2 Step 1 High threshold (Read & Write)

Bit	Name	R/W	Reset Value	Description
7:0	LM75_2 Step 1 High threshold	R/W	TBD	LM75b Step 1 High threshold temperature value with 2's complement.

1.2.64. Offset 0xC5 LM75_2 Step 2 Low threshold (Read & Write)

Bit	Name	R/W	Reset Value	Description
7:0	LM75_2 Step 2 Low	R/W	TBD	LM75b Step 2 Low threshold temperature value with

	threshold			2's complement.
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1.2.65. Offset 0xC6 LM75_2 Step 2 High threshold (Read & Write)

Bit	Name	R/W	Reset Value	Description
7:0	LM75_2 Step 2 High threshold	R/W	TBD	LM75b Step 2 High threshold temperature value with 2's complement.

1.2.66. Offset 0xC7 LM75_2 Max Low threshold (Read & Write)

Bit	Name	R/W	Reset Value	Description
7:0	LM75_2 Max Low threshold	R/W	TBD	LM75b Max Low threshold temperature value with 2's complement.

1.2.67. Offset 0xC8 LM75_3 Step 1 High threshold (Read & Write)

Bit	Name	R/W	Reset Value	Description
7:0	LM75_3 Step 1 High threshold	R/W	TBD	LM75c Step 1 High threshold temperature value with 2's complement.

1.2.68. Offset 0xC9 LM75_3 Step 2 Low threshold (Read & Write)

Bit	Name	R/W	Reset Value	Description
7:0	LM75_3 Step 2 Low threshold	R/W	TBD	LM75c Step 2 Low threshold temperature value with 2's complement.

1.2.69. Offset 0xCA LM75_3 Step 2 High threshold (Read & Write)

Bit	Name	R/W	Reset Value	Description
7:0	LM75_3 Step 2 High threshold	R/W	TBD	LM75c Step 2 High threshold temperature value with 2's complement.

1.2.70. Offset 0xCB LM75_3 Max Low threshold (Read & Write)

Bit	Name	R/W	Reset Value	Description
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7:0	LM75_3 Max Low threshold	R/W	TBD	LM75c Max Low threshold temperature value with 2's complement.
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1.2.71. Offset 0xCC LM75_4 Step 1 High threshold (Read & Write)

Bit	Name	R/W	Reset Value	Description
7:0	LM75_4 Step 1 High threshold	R/W	TBD	LM75d Step 1 High threshold temperature value with 2's complement.

1.2.72. Offset 0xCD LM75_4 Step 2 Low threshold (Read & Write)

Bit	Name	R/W	Reset Value	Description
7:0	LM75_4 Step 2 Low threshold	R/W	TBD	LM75d Step 2 Low threshold temperature value with 2's complement.

1.2.73. Offset 0xCE LM75_4 Step 2 High threshold (Read & Write)

Bit	Name	R/W	Reset Value	Description
7:0	LM75_4 Step 2 High threshold	R/W	TBD	LM75d Step 2 High threshold temperature value with 2's complement.

1.2.74. Offset 0xCF LM75_4 Max Low threshold (Read & Write)

Bit	Name	R/W	Reset Value	Description
7:0	LM75_4 Max Low threshold	R/W	TBD	LM75d Max Low threshold temperature value with 2's complement.

1.2.75. Offset 0xD0 TMP432_1 Step 1 High threshold (Read & Write)

Bit	Name	R/W	Reset Value	Description
7:0	TMP432_1 Step 1 High threshold	R/W	TBD	LM75d Step 1 High threshold temperature value with 2's complement.

1.2.76. Offset 0xD1 TMP432_1 Step 2 Low threshold (Read & Write)

Bit	Name	R/W	Reset Value	Description
7:0	TMP432_1 Step 2 Low threshold	R/W	TBD	LM75d Step 2 Low threshold temperature value with 2's complement.

1.2.77. Offset 0xD2 TMP432_1 Step 2 High threshold (Read & Write)

Bit	Name	R/W	Reset Value	Description
7:0	TMP432_1 Step 2 High threshold	R/W	TBD	LM75d Step 2 High threshold temperature value with 2's complement.

1.2.78. Offset 0xD3 TMP432_1 Max Low threshold (Read & Write)

Bit	Name	R/W	Reset Value	Description
7:0	TMP432_1 Max Low threshold	R/W	TBD	LM75d Max Low threshold temperature value with 2's complement.

1.2.79. Offset 0xD4 TMP432_2 Step 1 High threshold (Read & Write)

Bit	Name	R/W	Reset Value	Description
7:0	TMP432_2 Step 1 High threshold	R/W	TBD	LM75d Step 1 High threshold temperature value with 2's complement.

1.2.80. Offset 0xD5 TMP432_2 Step 2 Low threshold (Read & Write)

Bit	Name	R/W	Reset Value	Description
7:0	TMP432_2 Step 2 Low threshold	R/W	TBD	LM75d Step 2 Low threshold temperature value with 2's complement.

1.2.81. Offset 0xD6 TMP432_2 Step 2 High threshold (Read & Write)

Bit	Name	R/W	Reset Value	Description
7:0	TMP432_2 Step 2 High threshold	R/W	TBD	LM75d Step 2 High threshold temperature value with 2's complement.

1.2.82. Offset 0xD7 TMP432_2 Max Low threshold (Read & Write)

Bit	Name	R/W	Reset Value	Description
7:0	TMP432_2 Max Low threshold	R/W	TBD	LM75d Max Low threshold temperature value with 2's complement.

1.2.83. Offset 0xD8 TMP432_3 Step 1 High threshold (Read & Write)

Bit	Name	R/W	Reset Value	Description
7:0	TMP432_3 Step 1 High threshold	R/W	TBD	LM75d Step 1 High threshold temperature value with 2's complement.

1.2.84. Offset 0xD9 TMP432_3 Step 2 Low threshold (Read & Write)

Bit	Name	R/W	Reset Value	Description
7:0	TMP432_3 Step 2 Low threshold	R/W	TBD	LM75d Step 2 Low threshold temperature value with 2's complement.

1.2.85. Offset 0xDA TMP432_3 Step 2 High threshold (Read & Write)

Bit	Name	R/W	Reset Value	Description
7:0	TMP432_3 Step 2 High threshold	R/W	TBD	LM75d Step 2 High threshold temperature value with 2's complement.

1.2.86. Offset 0xDB TMP432_3 Max Low threshold (Read & Write)

Bit	Name	R/W	Reset Value	Description
7:0	TMP432_3 Max Low threshold	R/W	TBD	LM75d Max Low threshold temperature value with 2's complement.

1.3. CPLD pin-out list

1.3.1.Fan CPLD pin-out list

PIN	NET NAME	IN/ OUT	
B1	GPIO_1	IN	
D1	CPLD_TDO_A	OUT	
E1	CPLD_TDI_A	IN	
H1	CPLD_TCK_A	OUT	
H2	CPLD_TMS_A	IN	
H6	25MHZ_OUT_R	IN	
J1	FAN2_LED_G	OUT	
J2	FAN2_LED_R	OUT	
K1	FAN2_SENSOR_OUT	IN	
K2	FAN2_SENSOR_IN	IN	
L1	FAN2_PWM	OUT	
L2	EN_FAN2	OUT	
L3	TMP1_CLKOUT_P	IN	
M1	FAN2_PRESENT	IN	
M2	FAN1_LED_G	OUT	
M3	TMP1_CLKOUT_N	IN	
N2	FAN1_LED_R	OUT	
N3	FAN5_PWM	OUT	
L4	FAN7_PWM	OUT	
L5	FAN8_PWM	OUT	
L10	FAN5_LED_G	OUT	
L11	FAN5_LED_R	OUT	
M4	FAN1_SENSOR_IN	IN	
M5	FAN6_PWM	OUT	
M7	FAN1_PRESENT	IN	
M8	FAN8_LED_G	OUT	
M9	FAN6_SENSOR_IN	IN	
M10	FAN8_SENSOR_IN	IN	
M11	FAN5_SENSOR_IN	IN	
M12	EN_FAN6	OUT	

M13	FAN7_SENSOR_IN	IN	
N4	FAN1_SENSOR_OUT	IN	
N5	FAN1_PWM	OUT	
N6	EN_FAN1	OUT	
N7	FAN6_LED_G	OUT	
N8	FAN6_LED_R	OUT	
N9	FAN8_LED_R	OUT	
N10	FAN6_SENSOR_OUT	IN	
N11	FAN8_SENSOR_OUT	IN	
N12	FAN5_SENSOR_OUT	IN	
G12	FAN7_PRESENT	IN	
G13	FAN5_PRESENT	IN	
H13	FAN6_PRESENT	IN	
J12	FAN_SDA2_R	IN / OUT	
J13	FAN7_LED_R	OUT	
K11	FAN7_LED_G	OUT	
K12	FAN_SCL1_R	OUT	
K13	FAN_SCL2_R	OUT	
L12	FAN7_SENSOR_OUT	IN	
L13	FAN_SDA1_R	IN / OUT	
A12	FAN4_PRESENT	IN	
B11	FAN_SDA_1_R	IN / OUT	
B12	EN_FAN4	OUT	
B13	FAN4_SENSOR_IN	IN	
C11	FAN3_LED_G	OUT	
C12	FAN4_SENSOR_OUT	IN	
C13	FAN4_LED_R	OUT	
D11	FAN4_PWM	OUT	
D12	FAN4_LED_G	OUT	
D13	CPU_FAN_CPLD_RST_N	IN	
E12	EN_FAN7	OUT	
E13	EN_FAN5	OUT	
F12	FAN_INT_L	OUT	
F13	EN_FAN8	OUT	

G10	FAN8_PRESENT	IN	
A2	FAN3_PWM	OUT	
A3	FAN3_SENSOR_OUT	IN	
A4	EN_FAN3	OUT	
A7	CPU_UPGRADE_I2C_INT_L	IN	
A10	I2C_FAN_MNGMT_SCL	IN	
A11	FAN3_LED_R	OUT	
B2	FAN3_PRESENT	IN	
B3	FAN3_SENSOR_IN	IN	

Table 1-2 Fan board CPLD Pin-out Table